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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	15

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/394,011	BLACKMON ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed December 16, 2003 in response to PTO Office Action mailed September 10, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-21 have been presented for examination in this application. In response to the last Office Action, claim 1 has been amended. No claims have been canceled or added. As a result, claims 1-21 are now pending in this application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al (US6,385,708) and Harriman et al (US6,088,772) and Howe et al (US6,145,052).

As per claim 1, Stracovsky discloses a method for processing commands in a computer memory subsystem comprising (a) receiving a plurality of

commands on a bus network connected to said memory subsystem [*processor 102 generates memory address requests*; col. 6, lines 1-19]; (b) categorizing said received commands into command types [*interface 110 converts received command and address a universal command 200 which contains 5 data fields: pre-charge, activate, read, write, refresh*; col. 6, lines 30-43; col. 8, lines 22-24];

(d) determining memory cycle performance penalties of said categorized commands in each of said queues [*earliest issue time and data occurrence time associated with the commands are determined*; col. 3, lines 2-11]; (f) determining if each of said selected command is valid [*data occurrence time and durations of the command ready to be issued are compared with data occurrence time and durations previously issued commands to detect collisions*; col. 20, lines 11-28]; (g) arbitrating said valid commands and selecting one of said valid commands to execute [*when a command is issued, addresses for lower priority commands are shifted into higher priority positions*; *command with highest priority based on the comparison is issued*; col. 20, lines 34-50].

However, Stracovsky does not specifically teach (c) placing each received command into a queue pertaining to its respective command type; (e) reordering said categorized commands in each of said queues so that one categorized command in each of said queues having the least memory cycle performance penalty is selected for execution; and (h) executing sequential valid commands of the same command type as recited in the claim.

Harriman discloses (c) placing each received command into a queue pertaining to its respective command type [*command queue block has three separate command queues, a normal priority read queue 316, a normal priority write queue 318, and a*

high priority read or write queue 318; col. 4, lines 31-67]; (h) executing sequential valid commands of the same command type [*high priority data is returned in order*; col. 3, lines 21-25, col. 5, lines 65-66] to provide an adequate command reordering mechanism which balances latency and bandwidth concerns while optimizing based on performance criteria such as locality and/or command type (col. 2, lines 28-31).

Howe discloses reordering categorized commands in each of said queues so that one categorized command in each of said queues having the least memory cycle performance penalty is selected for execution [*commands are reordered based on a number of factors such as age of the command and mechanical time delay*; col. 1, lines 35-57] to beneficially ensure that commands received are efficiently completed within a given time period thus improving system performance (col. 3, lines 11-14).

It would have been obvious to one of ordinary skill in the art, having the teachings of Stracovsky and Harriman and Howe before him at the time the invention was made, to modify the system of Stracovsky to include placing each received command into a queue pertaining to its respective command type and executing sequential valid commands of the same command type because it was well know to benefit by provide an adequate command reordering mechanism which balances latency and bandwidth concerns while optimizing based on performance criteria such as locality and/or command type (col. 2, lines 28-31) as taught by Harriman; and to include reordering categorized commands in each of said queues so that one categorized command in each of said queues having

the least memory cycle performance penalty is selected for execution because it was well know to beneficially ensure that commands received are efficiently completed within a given time period thus improving system performance (col. 3, lines 11-14) as taught by Howe.

As per claim 2, Stracovsky discloses said command types are forms of store and fetch commands [col. 12, line 58].

As per claim 3, Stracovsky discloses said command types are associated with a particular source or destination of said received memory commands [col. 7, lines 61- col. 8, line 26].

As per claim 4, Stracovsky discloses said particular source or destination is a particular computer processor connected on said bus [col. 6, lines 7-10].

As per claim 5, the concept of a particular source or destination being an I/O hub controller functionally connected on a bus is well known in the state of the art.

As per claim 6, the concept of a particular source or destination being a switching fabric connected to a bus is well known in the state of the art.

As per claim 7, the concept of a particular source or destination being a compression/decompression engine functionally connected to a bus is well known in the state of the art.

As per claim 8, Stracovsky discloses said command types, which originate from or are required for a particular application have priority [col. 8, lines 30-33].

As per claim 9, Stracovsky discloses said step of receiving a plurality of commands further comprises determining if any of said received commands have an address dependency and passing said address dependency determination with said memory command [col. 6, lines 13-20].

As per claim 10, Stracovsky discloses said step of determining memory cycle performance penalties of said categorized commands further comprises comparing a number of oldest received categorized commands with each other [col. 20. lines 45-50].

As per claim 11, Stracovsky discloses said step of determining memory cycle performance penalties of said categorized commands further comprises comparing a number of oldest received categorized commands with a previously chosen command [col. 18, lines 1-7].

As per claim 12, Stracovsky discloses said step of determining memory cycle performance penalties of said categorized commands further comprises comparing a number of oldest received categorized commands with a previously chosen command [col. 20, lines 13-28].

As per claim 13, Stracovsky discloses said step of reordering said categorized commands further comprises selecting the oldest of said categorized commands that have the least memory cycle performance penalty for execution [col. 20, lines 45-50].

As per claim 14, Harriman discloses said step of arbitrating said reordered valid commands further comprises granting priority to said type of command having said least memory cycle performance penalty [col. 4, lines 2-5].

As per claim 15, Harriman discloses said step of arbitrating said reordered valid commands further comprises granting priority to a command type other than said command type of said reordered valid commands [col. 7, lines 20-24].

As per claim 16, Harriman discloses said step of executing sequential valid commands of the same command type further continues until a valid memory command of said command type is no longer available, or until a predetermined number has been executed, or until a memory command of another of said command types has higher priority [col. 3, lines 44-64].

Claim 17 is rejected as per claims 1, 2, 9-13 and 16 above.

Claim 18 is rejected as per claims 1 and 16 above.

Claim 21 is rejected as per claims 1, 11, 12, 13 and 16 above.

5. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al (US6,385,708) and Harris (US6,601,151) and Howe et al (US6,145,052).

As per claim 19, Stracovsky discloses a computer processing system comprising (a) a plurality of bus units [*elements 106*; Fig. 1A]; said bus units comprising at least one computer processor [*requesting device 102*; col. 6, line 2]; at least one I/O device [*element 108*; Fig. 1A]; at least one memory cache system connected to said at least one computer processor [*large number of resource tags would require large cache memory*; col. 10, lines 28-30]; said memory commands

categorized into types [*Read and Write commands*; col. 12, lines 56-65]; (b) at least one memory subsystem connected on a first bus to said plurality of bus units, said memory subsystem responsive to said memory commands [*memory 108 receives requests from processor 102*; col. 6, lines 1-19]; and further comprising (i) a memory controller connected to a command interface functionally connected to said first bus [*controller 104 coupled to system interface 110 coupled to system bus 106*; col. 6, lines 1-5, Fig. 1A, elements 104, 110, 106]; (ii) a plurality of memory chips configured into memory banks ; said memory chips architected into memory cards attached to at least one memory bus [*resource 108 is a multi-bank type memory device such as a multi-chip module*; *resource 108 is coupled to system bus 106*; Fig. 1A, col. 7, lines 35-38]; (iii) a plurality of command FIFO queues, each of said command FIFO queues associated with one of said command types into which said memory commands are categorized [*read buffer 1022 receives read commands and write buffer 1020 receives write commands*; Fig. 10, col. 18, lines 11-16]; (v) an arbitration logic circuit to output said memory commands of said determined command type having said least memory cycle performance penalty to said plurality of memory chips [*address shifter 1614 determines the priority of commands and highest priority command is issued*; Fig. 16, col. 20, lines 31-50].

However, although Stracovsky discloses a comparison logic circuit which determines which memory command types have the least memory cycle performance penalty [*queue element for which command issue time is zero*; col. 20, lines 12-30], the reference does not specifically teach a plurality of comparison logic circuits, each of said plurality of comparison logic circuits associated with each of

said plurality of command FIFO queues; and an arbitration logic circuit to output said memory commands of said determined command type having said least memory cycle performance penalty to said plurality of memory chips as recited in the claim.

Harris discloses a plurality of comparison logic circuits, each of said plurality of comparison logic circuits associated with each of said plurality of command FIFO queues [*comparison logics 45 and 145 associated with read and write queues 30 and 130*; Fig. 9; col. 10, line 50 – col. 11, line 17].

Howe discloses reordering categorized commands in each of said queues so that one categorized command in each of said queues having the least memory cycle performance penalty is selected for execution [*commands are reordered based on a number of factors such as age of the command and mechanical time delay*; col. 1, lines 35-57] to beneficially ensure that commands received are efficiently completed within a given time period thus improving system performance (col. 3, lines 11-14).

It would have been obvious to one of ordinary skill in the art, having the teachings of Stracovsky and Harris and Howe before him at the time the invention was made, to modify the system of Stracovsky to include a plurality of comparison logic circuits, each of said plurality of comparison logic circuits associated with each of said plurality of command FIFO queues because it was well known to benefit by improving system efficiency by providing separate queues and associated logic blocks for reads and writes so that the logic blocks

can be tailored specifically to the memory access request type [col. 11, lines 8-11] as taught by Harris; and to include reordering categorized commands in each of said queues so that one categorized command in each of said queues having the least memory cycle performance penalty is selected for execution because it was well know to beneficially ensure that commands received are efficiently completed within a given time period thus improving system performance (col. 3, lines 11-14) as taught by Howe.

As per claim 20, Stracovsky discloses said comparison logic circuit further determines the oldest of said memory commands in each of said plurality of command FIFO queues [*queue element with highest priority (e.g., the oldest one) is issued*; col. 19, lines 65-67].

Response to Arguments

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach command reordering and granting priority to commands having least memory cycle performance penalty.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre M. Vital
Art Unit 2188
February 4, 2004